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1. Introduction

SmartCtrl\(^1\) is a general-purpose controller design software specifically for power electronics application. This tutorial is intended to guide you, step by step, to design the digital control loop of a buck converter and simulate it with PSIM.

2. Digital Control Design

The Digital control feature is only available in the SmartCtrl 2.1 Pro. The design procedure begins with the design of the analog control loop. After that, the analog regulator is translated into the digital domain taking into account several specific parameters of the digital design.

The first step is to select the power converter and the type of control, i.e., the plant to be controlled. In this case, it is a voltage mode controlled Buck converter (Figure 1).

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The **second step** is to introduce the data corresponding to the plant, sensor and compensator. First, plant parameters are defined (Figure 2).

![Figure 2 Plant parameters dialog box.](image)

Sensor parameters are defined in the corresponding dialog box (Figure 3). When a digital control loop is designed, only “Voltage Divider” sensor must be selected.
After selecting the regulator type (Type 3, Type 2 or PI), a new dialog box appears (Figure 4). Modulator parameters are defined in this dialog box. Trailing edge unity gain modulator is selected for this case ($V_p=1$, $V_v=0$, $tr=10\mu s$).

**Figure 3 Sensor parameters dialog box**

**Figure 4 Regulator dialog box. Modulator parameters.**
The third step is to select the requirements of the control loop, i.e., to define the required cross over frequency of the open loop transfer function $f_c$ and the phase margin $PM$. In SmartCtrl the user can select graphically a solution inside the stable design space, called Solution Map (Figure 5), which defines the set of $(f_c, PM)$ resulting in a stable design. In this case, the selected cross over frequency is $f_c=4.5$ kHz, and the selected phase margin is $PM=50^\circ$.

The analog loop is already designed (Figure 6). The Bode plot and Nyquist plot can be used to analyze the stability, and the transient plot can be used to check the time domain performance. Once the analog regulator has been determined, the digital control capability of SmartCtrl 2.0 can be used to calculate the digital regulator. The procedure implemented in the Digital Control Module (Version 1.0) consist on converting the analog design in a digital regulator by means of discretization (bilinear transformation) of the analog regulator, taking into account some additional aspects of digital control.
Figure 6 Graphs corresponding to the analog regulator design.

The **fourth step** is to find the digital regulator, which can be calculated only after completing the design steps of an analog regulator. In the icon bar, the user can find the icon (Figure 7) to open the Digital settings dialog box. It can also be opened through the menu "Design->Digital Control".

Figure 7 Icon to open the “Digital control settings” dialog box
The digital settings box appears, asking for the specific digital parameters (Figure 9): sampling frequency, bits number and accumulated delay. The sampling frequency is often the same as the switching frequency, but it can be different. Note that the sampling frequency must be a multiple or submultiple of the switching frequency.

The bits number is related with the rounding of coefficients of digital compensator. Depending on each case, a different number of bits can be enough to obtain a digital regulator similar to analog regulator, as it will be detailed later. Note that bits number is referred only to the regulator coefficients calculation.

Accumulated delay is the time between the sampling instant and the PWM pulse effective updating (Figure 8), which is the falling edge in the trailing edge pulse width modulator. Therefore, accumulated delay includes analog to digital conversion delay, calculations delay and modulator delay, i.e., the sum of all delays in the digital control loop. In general, the sampling instant may not be the initial instant of the PWM period, as in this case.
When digital settings have been completed, the check box “Calculate digital compensator” must be checked. Then, the digital regulator is calculated, and icons to represent transfer function involving the digital regulator are enabled (Figure 10).

Digital factors sweep dialog box (Figure 11) allows for changing dynamically the digital settings and evaluate graphically the results. In the example of Figure 11 the number of bits has been changed, and the results corresponding to 6 bits are shown. As it can be seen, digital open loop and analog open loop transfer functions are different in magnitude (low frequencies) and in phase (medium and high frequencies). It means that the selected number of bits is not enough to represent the coefficients of the digital regulator, as it is the case of Figure 10, where 10 bits were selected. Note that in Figure 10 the magnitude of analog and digital responses are very similar, and phase responses are also very similar except in high frequency range. Note that digital and analog regulators are different near of the half of sampling frequency, regardless the selected number of bits, and the digital response takes into account the accumulated delay, which is not included in the analog transfer functions.
Figure 10 Graphs corresponding to analog and digital design. In the icon bar, the icon to represent the digital open loop gain $T_z$ is highlighted.
Once the digital regulator has been calculated, the entire design can be exported to PSIM, and then simulated (fifth step). In Figure 12 it is shown the corresponding icon. When clicking this icon, the export dialog box appears (Figure 13). In order to simulate the digital regulator, “z-domain coefficients” must be selected.
The design is exported to a PSIM schematic, including a file where all converter and controller parameters are contained.
Figure 14 PSIM schematic result of the exportation of a SmartCtrl design (digital regulator)

In the PSIM schematic the power stage and the digital control stage appear. A trailing edge pulse width modulator is included. In this particular implementation, the modulator introduces a time delay equal to $D/f_{sw}$, where $D$ is duty cycle corresponding to the steady state operating point, and $f_{sw}$ is the switching frequency. A “time delay” block is added to take into account the additional time delays in the control loop, in such a way that the total time delay in control loop is equal to the value of “accumulated delay” introduced by the user. The value of this “time delay” is automatically calculated by SmartCtrl.
A first test is to perform a time domain simulation to check that the steady state operating point is achieved, i.e., output voltage equal to 4 V in this case (Figure 15). Note that in this first test a long enough time simulation must be selected, in order to achieve steady state operation.

![Time domain simulation](image)

**Figure 15** Time domain simulation. Steady state operation is achieved.

The **sixth step** to simulate and compare the digital regulator is to include in the PSIM schematic the components to perform an AC sweep to calculate the open loop transfer function (Tz) with PSIM. These components are detailed in Figure 16. The result of the simulation is shown in Figure 17.
Figure 16 Blocks to be added to perform an AC Sweep in order to obtain the open loop transfer function $T_z$

Figure 17 Result of the PSIM AC Sweep
In order to compare the obtained AC response and the theoretical calculated with SmartCtrl, the digital transfer function data must be exported to a text file. In Figure 18 the menu to export the aforementioned data is shown. In Figure 19 the digital open loop transfer function export dialog box is shown. The parameters have been selected in order to be similar to the AC sweep parameters selected in PSIM (Figure 16).

![Figure 18 Exportation of the digital open loop transfer function from SmartCtrl to a text file](image-url)
Once SmartCtrl data have been exported to a text file, it has to be open, and the name of the first column must be changed by the name “Frequency”, in order to be merged in Simview and compared with PSIM simulation results. In Figure 20 digital open loop transfer function calculated with SmartCtrl and AC sweep simulation performed with PSIM are compared. The results of PSIM simulations and SmartCtrl calculations match well in this case.
Figure 20 Comparison of AC Sweep results simulated with PSIM (red) and SmartCtrl data (blue) for the open loop transfer function.
SmartCtrl includes also the capability to import data from text files and compare them with the transfer functions calculated in SmartCtrl. In File menu, option Import (Figure 21), a new dialog box “Functions to be merged” appears (Figure 22). In this dialog box, the user should select “Add”, and then the “Add transfer function” dialog box appears. Selecting T(f) button and clicking on “Text file”, will result in a new dialog box, "Load file containing transfer function to be compared", where the user will select the .fra file from the simulation with PSIM.

Finally, analog calculated, digital calculated and digital simulated transfer functions can be compared in the same Bode plot (Figure 23), where a good agreement between simulated and calculated digital open loop transfer functions can be observed.
Figure 23 Comparison between analog calculated, digital calculated and digital simulated open loop transfer functions.