Boost PFC Converter Control Loop Design

Tutorial – April 2016-
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1. Introduction

SmartCtrl\textsuperscript{1} is a general-purpose controller design software specifically for power electronics applications. This tutorial is intended to guide you, step by step, to design the control loops of a PFC (power factor correction) boost converter with the SmartCtrl Software.

The example used in this tutorial is the PFC boost converter circuit that comes with the PSIM example set. The PSIM schematic is shown in Figure 1.

![Schematic of the PFC boost converter circuit](image)

**Figure 1**

The circuit includes the inner current loop and the outer voltage loop. The current loop regulator parameters are the resistance $R_{cz}$ and the capacitances $C_{cz}$ and $C_{cp}$, and the voltage regulator parameters are the resistance $RV_{F}$ and the capacitance $CV_{F}$, highlighted in the red dotted boxes above.

\textsuperscript{1}SmartCtrl is copyright in 2009-2011 by Carlos III University of Madrid, GSEP Power Electronics Systems Group, Spain
Let's assume that these values are unknown. The objective is to design the current/voltage regulators using the SmartCtrl software. The design procedure is described below.

To begin the design process, in SmartCtrl, click on the icon, or from the Design menu, select Predefined topologies -> AC/DC converters -> PFC Boost converter.

The dialog window will appear as shown in Figure 2.

![Figure 2](image)

The PFC boost converter is controlled by a double loop control scheme. The inner loop is a current loop, and the outer loop is a voltage loop. Note that the PFC boost converter design must be carried out sequentially. The SmartCtrl program will guide you through this process.
2. Inner Loop Design

Before designing the inner loop, select the type of the multiplier.

1. **Select the Multiplier** *(Figure 3)*

   ![Figure 3](image)

   *Figure 3*

   In this case, select the UC3854A according to the schematic circuit.

   Attending to the schematic in Figure 1, the parameters of the multiplier for this particular example are the ones shown in Figure 4. Notice that \( K_{FF} \), the feed-forward gain, is the ratio between the rms input voltage and the average input voltage to the multiplier. It has been calculated applying (1):

   \[
   K_{FF} = \sqrt{2} \cdot \frac{2}{\pi} \cdot \frac{RFF_3}{RFF_1+RFF_2+RFF_3} \tag{1}
   \]

   \( RFF_1, RFF_2, RFF_3, Rac \) y \( Rmo \) are the resistances with the same name in the schematic in Figure 1.
2. **Select the gain of the inner loop sensor** (Figure 5)

Select a constant gain election of the current sensor Rs. It is a resistor and it is represented in the picture of the power plant (Figure 8).
So, the general graphic is Figure 6:

![Figure 6]

3. **Select the plant** (Figure 7).

![Figure 7]
Select the plant as **Boost PFC (Resistive load)** for boost PFC converter with the current loop and the voltage loop. Complete the parameters in the corresponding input data window (*Figure 8*). Note that the input voltage is the rms value.

For the design of the current loop, the plant is calculated as a DC/DC converter for a certain operating point, that is specified in the line angle \(\text{wta}(\degree)\).

When finished, click OK to continue.

*Figure 8*
4. Select the current regulator *(Figure 9).*

*Figure 9*

From the inner loop regulator drop-down menu, select “Type 2” as the current regulator type. It is necessary to know the ramp waveform in order to specify the parameters \(V_{\text{max}}\) (maximum voltage), \(V_{\text{min}}\) (minimum voltage) and \(tr\) (rise time). The parameters in *Figure 10* correspond to the simulation of the schematic in *Figure 9*, which provides the ramp waveform depicted in *Figure 11.*
Figure 10

![Diagram of Type 2 Boost PFC Converter Control Loop Design]

- $R_{1}(\text{ohms}) = 10k$
- $V_p(V) = 6.56$
- $V_m(V) = 1.055$
- $t_r(s) = 8.5u$
- $F_{sw}(Hz) = 100k$
- $T_{sw}(\mu s) = 18 u$

- $V_{ramp}$
- $V_{max}(V) = 6.56$
- $V_{min}(V) = 750m$
- $t_r(s) = 8.5u$

¡Error! No se encuentra el origen de la referencia.
5. Select the crossover frequency and the phase margin (Figure 11).

**Figure 11**

SmartCtrl provides a guideline and an easy way of selecting the crossover frequency and the phase margin through the **Solution Map.** Click on the **Set** button, and the Solution Map will be shown (Figure 12).
In the Solution Map, each point within the white area corresponds to a combination of the crossover frequency and the phase margin that leads to a stable solution. In addition, when a point is selected, the attenuation given by the sensor and the regulator at the switching frequency is provided.

To carry out the selection, left click a point within the white area, or enter the crossover frequency and the phase margin manually.

Once the crossover frequency and the phase margin are selected, the Solution Map will be shown on the right side of the converter input window. If, at any time, it is required to change the crossover frequency or the phase margin, click on the white area of the Solution Map, as shown in Figure 11.

**Figure 12**
Figure 13
3. Outer Loop Design

The procedure of designing the outer loop is similar to that of the inner loop design.

1. **Select the voltage sensor** *(Figure 14)*

   ![Figure 14](image_url)

   When using a voltage divider, one must enter the reference voltage, and the program will automatically calculate the sensor gain.

   However, in this particular example, the option is a “Regulator embedded voltage divider”.
2. Select the voltage regulator (Figure 15)

In this example, the regulator type is a “Single pole_unatt”, with the parameters specified in Figure 16. The reference voltage provided by the UC3854 is 7.5 V.
3. Determine the crossover frequency and the phase margin (Figure 17)
The crossover frequency and the phase margin of the outer loop must be selected. A Solution Map is also provided to help select a stable solution. Press the Solution map (outer loop) button and the solution map will appear (Figure 18). Then select a point by clicking within the white area, and click OK to continue.

![Solution Map](image)

**Figure 18**

Once the crossover frequency and the phase margin are selected, the Solution Map will appear on the right side of the converter input window. If, at any time, these two parameters need to be changed, click in the white area of the Solution Map, as shown in Figure 19.
Accept the selected design by clicking on OK. The program will automatically show the control system performance by means of the Bode plots, the Nyquist plot, phase margin, etc.

4. Design results

SmartCtrl provides the regulator component values needed to implement the regulators, as well as the voltage divider resistors (“Output data” in Figure 20). Since there are two control loops, one must select which one to display (Figure 20).
The Bode plots and Nyquist plot corresponding to the outer loop are shown in Figure 21, as well as the graphical information regarding the inner loop is shown in Figure 22. In the right panel “Method”, two parameters appear:

- Attenuation \((f_{sw}) (\text{dB})\). This is the attenuation in dB achieved by the open loop transfer function at the switching frequency. It should be low for the inner loop and the outer loop.

- Loop gain \((2f_l)(\text{dB})\). This is the attenuation in dB achieved by the open loop transfer function at twice the line frequency (100 Hz or 120 Hz). It should be high for the inner loop and low for the outer loop.

By clicking with the right button on the line current panel, a floating menu appears, offering different choices. One of them is the command FFT, which displays a new window with a plot that shows the amplitude of the first and third harmonics of the line current, to provide more information regarding the harmonic distortion.
Figure 21

Figure 22
The red dot in the rectified line voltage plot (Figure 22) originally corresponds to the line angle wta specified in the plant window (Figure 8). This dot can be moved by clicking and dragging, and the Bode plot and the attenuation parameters will refresh, as the plant is recalculated considering the equivalent DC/DC converter for that particular operating point. An example is depicted in Figure 23, modifying the line angle. Notice how the open-loop gain varies.
The blue dot in the rectified line voltage plot (Figure 22) is placed in the line angle that corresponds to the maximum current ripple through the inductor. Some results obtained by simulating the schematic in Figure 1 are depicted in Figure 24, to illustrate the meaning of this blue dot. In the left part of Figure 24, the voltage at the output of the rectifier and the current through the inductor are shown, indicating the position of the blue dot. In the right part of the figure, a detail of the same waveforms is shown, as well as the oscillator ramp and the internal compensator output. PSIM results (lower part of Figure 24) can be compared with SmartCrtl results for the same line angle.

The plot that shows the oscillator ramp and the inner compensator output is useful to determine whether there could be oscillations. If the slopes of both
functions are too similar, there could be more than one intersection per period, causing oscillations.

Figure 24
When a single-pole is used as the compensator type of the outer loop, there are some advantages regarding the line current distortion. On the other hand, the actual output voltage may not be exactly the specified due to the low gain at low frequency (see Bode plot gain in Figure 21), causing some differences between the SmartCtrl results and the simulated results. However, if the actual output voltage is 10% higher than the specified one, SmartCtrl will provide a warning message, recommending the user to check this point and increase low frequency gain. In this particular example, the actual output voltage is 415 V instead the specified 400 V, and consequently there is not any warning message.

**Table 1**

<table>
<thead>
<tr>
<th>Original design</th>
<th>New design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inner loop (type 2)</td>
<td>Inner loop (type 2)</td>
</tr>
<tr>
<td>fc=15 kHz</td>
<td>fc=15 kHz</td>
</tr>
<tr>
<td>PM=60º</td>
<td>PM=60º</td>
</tr>
<tr>
<td>Outer loop (single-pole)</td>
<td>Outer loop (single-pole)</td>
</tr>
<tr>
<td>fc=25 Hz</td>
<td>fc=15 Hz</td>
</tr>
<tr>
<td>PM=40º</td>
<td>PM=60º</td>
</tr>
<tr>
<td>Specified output voltage</td>
<td>Specified output voltage</td>
</tr>
<tr>
<td>400 V</td>
<td>400 V</td>
</tr>
<tr>
<td>Actual output voltage</td>
<td>Actual output voltage</td>
</tr>
<tr>
<td>415 V</td>
<td>448 V</td>
</tr>
</tbody>
</table>
To illustrate this problem related with the low gain of the outer loop at low frequency, a new outer loop has been designed, with different phase margin (PM) and cross-over frequency (fc). The comparison between this design and the original one can be found in Table 1. The new design has a lower gain at low frequency and the measured output voltage is 448 V, that is, more than 10% higher than the specified value.

Regarding the inner control loop, it is very important to consider that it is necessary to have a high enough bandwidth in order to follow the rectified sinusoidal reference. If the cross-frequency of the current loop is not high enough, a zero-crossing distortion in the input current will happen. In these occasions, the results provided by SmartCtrl may not match the actual results, as the line current
The waveform is calculated by SmartCtrl assuming that the current loop follows perfectly well the reference generated by the outer loop. Consequently, when a zero-crossing distortion is expected, the program displays a warning message to inform the user that the actual line current would differ from the one represented. The cross-frequency of the inner loop compensator should be increased to minimize this problem.

To illustrate this problem related with the low cross-over frequency of the inner loop, a comparison between several designs of the inner loop with different phase margin (PM) and cross-over frequency (fc). The input current waveforms achieved with these designs are compared in ![Error! No se encuentra el origen de la referencia.](#). Notice the important zero-crossing distortion for cross-over frequency lower than 5 kHz, and how the distortion is minimized as the cross-frequency is increased.